MICROMACHINED STIMULATING ELECTRODES

Quarterly Report #4

(Contract NIH-NINDS-N01-NS-5-2335)

July 1996 --- September 1996

Submitted to the

Neural Prosthesis Program
National Institute of Neurological Disorders and Stroke
National Institutes of Health

by the

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Department of Electrical Engineering and Computer Science
University of Michigan
Ann Arbor, Michigan
48109-2122

October 1996

MICROMACHINED STIMULATING ELECTRODES

Summary

During the past quarter, work in this program has gone forward in several areas. We have continued to fabricate passive probe structures for internal and external users. These probes have used the new site design, which allows the site to overlap adjacent conductors and permits a thorough cleaning step after via formation and before metal. Passive probes have been successfully fabricated using an external foundry (MCNC, Research Triangle Park, NC) as an effort to improve yield on devices where the fabrication process and designs are fully developed. The resulting probes appear very good, with dielectric stresses near neutral and interconnects well defined and defect free.

Results of in-vivo site pulsing have been interpreted in terms of an equivalent circuit model, focusing on the range between 100Hz and 10kHz. The impedance magnitude spectra agrees well with the model. Changes due to current pulsing can be correctly modeled in terms of the charge-transfer (redox) reactions thought to occur within the iridium oxide. It is theorized that current pulsing improves electrolyte access to the interface, thereby facilitating the oxidation/reduction reactions in the iridium oxide. This hypothesis is supported by *in vitro* tests that show no change in impedance when an electrode is pulsed in PBS. Encapsulation can be observed in these impedance spectra and has a significant effect on impedance during the first two weeks of implantation. CV testing can partially reverse these impedance increases, implying, for example, that the ability to stimulate recording probes to improve their electrolyte access should be beneficial. The impedance spectra of the new site structure are not significantly different than those of the older structure, although anomalous open circuit potentials have been observed on some sites and are being studied.

The use of TiN plugs in circuit vias has been successful. These Si-Ti-TiN-Al contacts showed resistances of approximately 7.5Ω for 4μm x 4μm contacts and 10Ω for 3μm x 3μm contacts, which is not noticeably higher than resistances measured for contacts containing no diffusion barrier. Additionally, after the wafers were then annealed for 2 hours at 425°C (the temperature and approximate time required for a 1μm low-temperature oxide (LTO) deposition), the contact resistances remained low, demonstrating that LTO may be used as a top dielectric over this type of interconnect without any negative effects on the contact properties. $TaSi_2$ has also been explored as an interconnect in areas requiring high-temperature probe upper dielectrics (e.g., on probe shanks). This material has been found to allow resistances of about 2.2 ohms/square (five times less than polysilicon) and is able to withstand temperatures of up to 950°C, consistent with the use of stoichiometric LPCVD oxide and nitride top dielectrics.

Studies of contact formation etch techniques have concluded that the use of RIE plus either an oxygen plasma or a piranha etch to remove residual polymers can produce high-quality contacts over both n- and p-type silicon and polysilicon areas. The use of RIE alone or RIE plus BHF or other chemical cleaning agents has not been found to be acceptable with all surfaces to be contacted. Work on the development of active probes is continuing and will use these new contact and interconnect structures. A new run of STIM-1A, -1B, and -2 probes is now underway. In addition, the layout of STIM-2B, a four-channel 64 site probe with off-chip current generation, is nearing completion.

MICROMACHINED STIMULATING ELECTRODES

1. Introduction

The goal of this research is the development of active multichannel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully and distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be demultiplexed on the probe to provide access to a large number of stimulating sites. Our goal in this area has been to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes which are then applied to the tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in our previous reports, we are now developing a series of active probes containing CMOS signal processing electronics. Two of these probes are slightly redesigned versions of an earlier first-generation set of designs and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is a second-generation version of our high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in setting the per-channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while -1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-1B is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to stimulation. A new probe, STIM-2B, is currently being added to this set. It offers 64-site capability with off-chip generation of the stimulus currents on four separate channels.

During the past quarter, we have continued to fabricate passive probe structures for internal and external users. Passive probes have been fabricated in an external foundry for the first time. We have also continued detailed characterization studies of chronically-implanted stimulating sites, interpreting the results in terms of an equivalent circuit model.

Technology studies aimed at the development of low-resistance interconnect structures and low-resistance circuit contacts for active probes have continued, along with fabrication of STIM-1A/B and the design of STIM-2B. The results in each of these areas are described below.

2. *Passive Probe Fabrication*

During the past quarter, work on the fabrication of passive probes has continued. We have completed three fabrication runs yielding probes for a variety of physiologists using these structures in their research. Probe characteristics from most of these wafers were as desired. Resistances were ohmic without adhesion or barrier problems and the sites activated normally. It is to be noted that these probes for the most part have used our new site configuration as shown in Fig. 1 below. This configuration is non-self-aligned and permits a vigorous cleaning of the silicon surface prior to site metal deposition. It also permits the site to overlap adjacent conductors in order to conserve probe width.

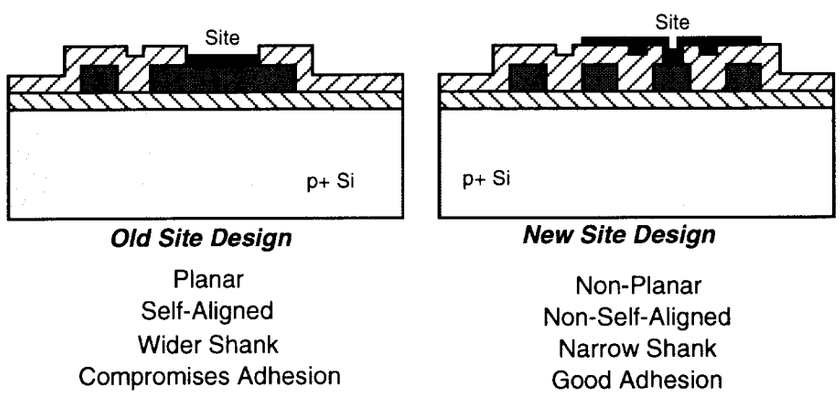

Fig. 1: Comparison of old (self-aligned) and new (non-self-aligned) site options.

A concern in the new site design is the large step between the top of the stacked oxide-nitride dielectrics on the shanks (and over the interconnect) and the interconnect surface. At the upper edge of such steps the deposited Ir is apt to be thinner than over the flat portions of the site; however, SEM investigations have shown no breaks in such areas. Abnormal open-circuit site potentials have been observed on some of these sites by ourselves and others, but it is not yet clear why this occurs. Certainly no polysilicon could be exposed during the final probe micromachining etch since it would be vigorously attacked by the EDP, causing a catestrophic failure of the device. These abnormalities will be the focus of studies during the coming quarter as discussed further below. Figure 2 shows a stepped-site option that is also possible at contacts that would reduce the step height. The upper oxide is first opened using a larger mask via and the dielectrics are removed down to the lower oxide layer using wet and/or dry etching. A smaller mask is then used to open the lower oxide. Thus, the transition is made in two steps. This also somewhat simplifies the contact etching, since an all wet process is possible as well as a thorough cleaning step prior to the final oxide opening. A final wet etch of the lower oxide is possible without the "cave" created in previous processes. It is to be stressed that it is not clear that such contact options are needed. The present processes appear to be working satisfactorily in most respects. However, it is important that these contacts can be engineered to overcome problems once those problems are identified and understood.

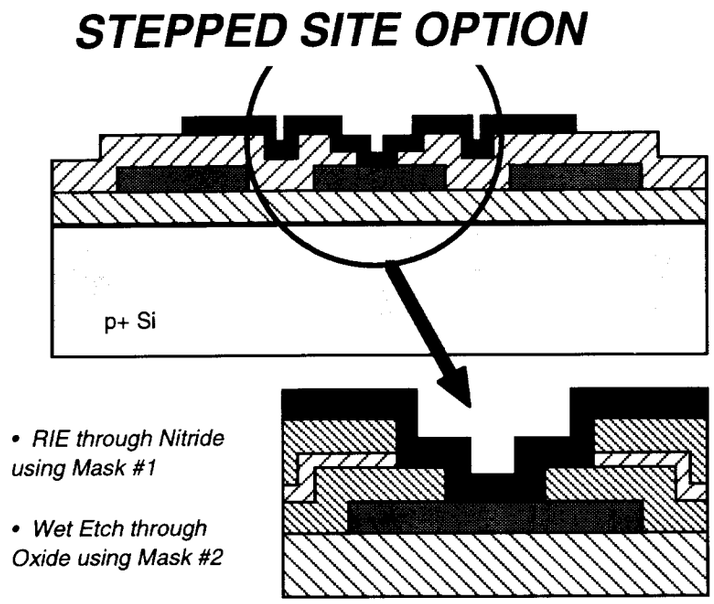

Fig. 2: Optional site contact arrangement for producing stepped sites opened in a two-mask process to reduce step coverage requirements over the dielectrics.

It should also be noted that during the last quarter, the first passive probes were successfully fabricated in an outside foundry. This is very significant in terms of expected probe yield. The probes were run at MCNC and appear to have very high yield along with consistent characteristics. MCNC performed all processing steps with the exception of the deep boron diffusion and the iridium site definition, which were performed at Michigan. Using permanent staff to fabricate the probes in a facility not open to other users affords the additional control not available in a university laboratory to permit the yields desired from a process aimed at satisfying the needs of external users. We were particularly pleased that the dielectric stresses were very well controlled in this process and that the polysilicon interconnects are well defined and defect free. Additional probes will be fabricated and evaluated using this approach in coming quarters by the Center for Neural Communication Technology at Michigan.

3. *Iridium Site Studies*

Three activities are reported in connection with studies of iridium sites during the present period: 1) Experimental data on the states of electrode sites during a period of daily stimulation (reported last quarter) was used to verify the form of a circuit model of the metal/media interface and to estimate model parameters; 2) An experiment was done to examine the effects of post-operative healing and encapsulation on the electrical characteristics of the electrode; and 3) The new site structure was tested *in vitro*.

Model Studies

Data taken previously during pulse experiments conducted over periods of one week were examined rigorously in the context of accepted models of electrode/media interfaces.

The Experiments-

Chronic experiments were run to measure the *in vivo* effects of electrical stimulation on the electrical parameters of the electrode-tissue interface. These experiments were reported last quarter and the protocol and data will be reviewed briefly here.

A chronic stimulating electrode was implanted in the cortex of a guinea pig using methods previously described. The electrodes consisted of 6 or 8 sites of varying size ($400\mu m^2$ to $1600\mu m^2$). Stimulation began after a 10-17 day recovery period. Biphasic current pulses (variable magnitude, 100μsec/phase, 250pulses/sec) were applied monopolarly for two hours on five consecutive days. (Previous experiments stimulated for four hours, but results from those experiments showed that impedance changes usually occur during the first few minutes of pulsing. The stimulation time was shortened to two hours so that more sites could be tested in one day. Two hours is a sufficient amount of time to produce a change in the impedance and still accumulate a significant number of pulses, 1.8 million per day.) Impedance spectroscopy (IS) and cyclic voltammetry (CV) data were collected on each stimulated site and on one unstimulated control site during the week, before and after the two hours of stimulation. The measurement system included a potentiostat (EG&G 283), a frequency response analyzer (EG&G 1025), and a 486 PC. The test cell consisted of the activated iridium stimulation site (working) and two 316 stainless steel head screws (counter and reference).

Results for two days of an experiment are shown in Figs. 3 and 4. The section of the spectrum on which the analysis is focused is the frequency range from 100Hz to 100kHz. This area exhibits a transient change in impedance that is correlated to current pulsing.

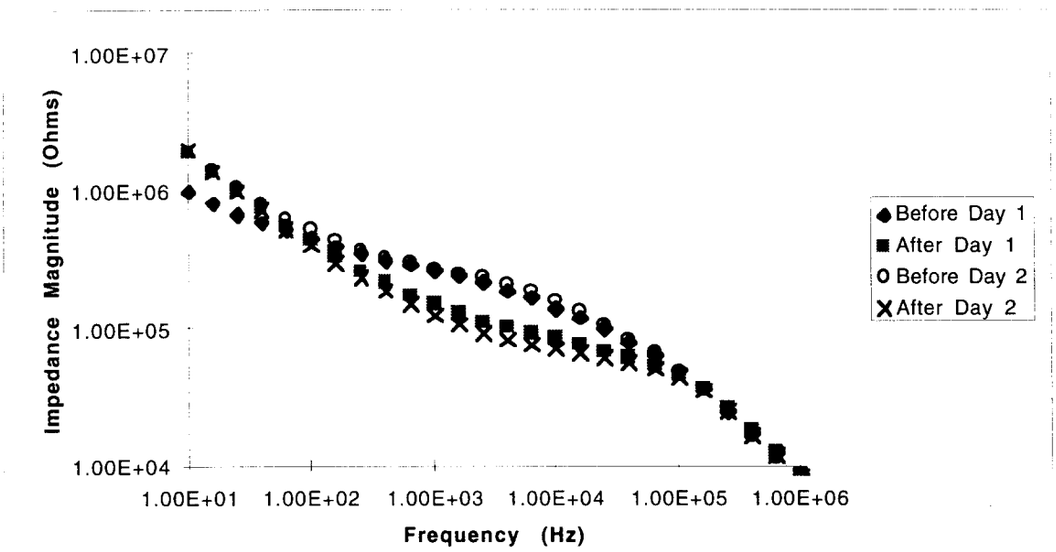

Fig. 3: *In vivo* impedance magnitude for two days of stimulation.

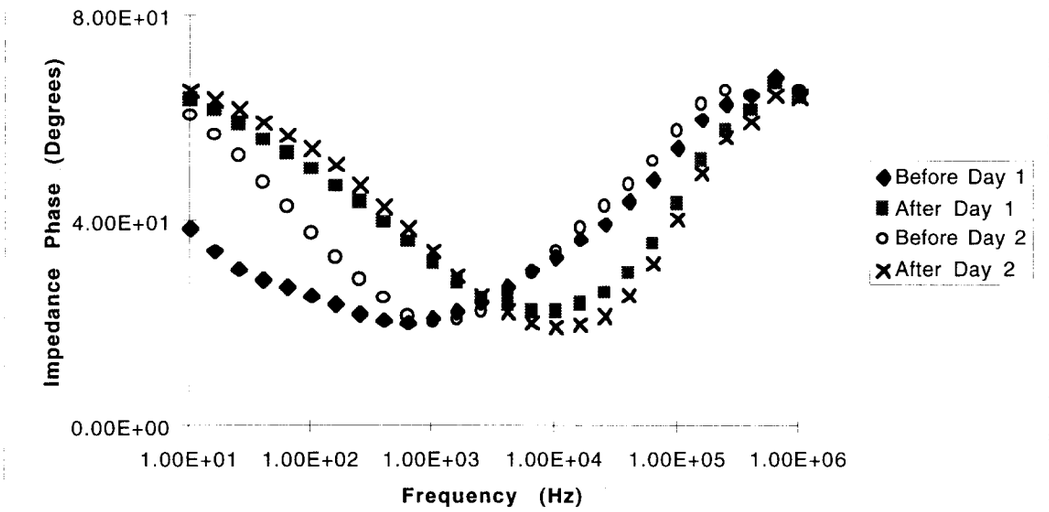

Fig. 4: *In vivo* impedance phase for two days of stimulation

Model Calculations-

A circuit model of the iridium oxide interface is shown below (Fig. 5). R_s is the resistance of electrolyte, cabling, etc. C_{dl} is the capacitance of the double layer. The charge transfer reaction in the iridium oxide is represented by R_{ct}. The impedance of ion diffusion through the iridium oxide is represented by a constant phase element CPE. This is a simplified model compared to the one in last quarter's report. The new model was recently proposed by investigators at EIC. The CPE is similar to a Warburg impedance for a transmission line. A true Warburg will have a phase of 45°, which represents semi-infinite diffusion to the interface. Our phase in the low frequency region was usually around 70°. This discrepancy is due to the thickness of the iridium oxide. A thin oxide does not meet the semi-infinite length required for Warburg diffusion[1].

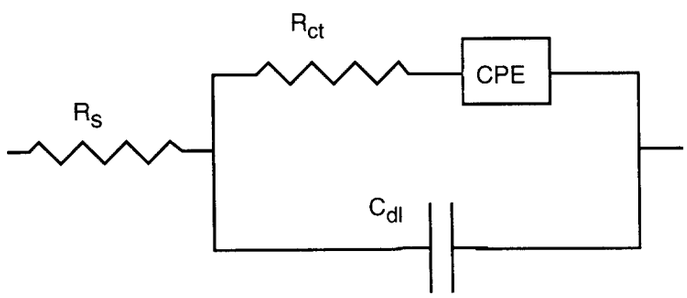

Fig. 5: Circuit Model of Iridium Oxide

[1]U. Twardoch, EIC Laboratories, personal conversation.

The impedance magnitude spectra fit the model fairly well. The sloped region at high frequency is the capacitive double layer charging (Fig. 3). C_{dl} is small so it already has a significant impedance at 1MHz. The flat region between 100Hz and 50kHz is due to charge transfer via the oxidation/reduction of the iridium oxide. The constant phase behavior (Fig. 6) of the iridium oxide takes over at low frequencies. The portion of the model that exhibits transient changes due to stimulation (Fig. 3) is related to the redox reactions within the iridium oxide and is represented by R_{ct}.

Another way to look at the impedance is to plot is Z_{real} vs. $-Z_{imag}$ (i.e., plot the data in the impedance plane) (Fig. 7). This representation is most useful when fitting experimental data to predicted data (from a circuit model). The modeling procedure uses the "impedance locus" to graphically estimate the values of the circuit model elements. An idealized example will be used to explain the procedure. Simulated data from a simplified interface model (Fig. 6) is plotted in the impedance plane (Fig. 7). The data forms a semicircle, with frequency increasing as the points approach the origin. While the data never actually intercept the real axis (except mathematically at infinite frequency and DC), the semicircle can be extended down to the real axis. The intercept nearest the origin (very high frequency, C_{dl} a short circuit) gives the value of R_s. The intercept further away from the origin (DC, C_{dl} an open circuit) equals R_{ct} plus R_s. With R_{ct} and R_s known, one can estimate C_{dl} from the frequency at the peak of the semicircle.

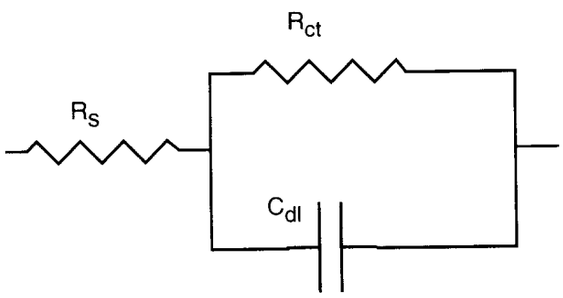

Fig. 6: Simplified circuit model.

Real data, of course, does not produce such perfect geometries in the imaginary plane. However, it is possible to graphically estimate circuit parameters from real data and then use an iterative curve fitting routine to match a model to the data. The impedance locus in Fig. 8 exhibits the semicircle associated with the high frequency portion of the model (R_s, R_{ct}, C_{dl}) as well as a straight line trajectory which is attributable to the CPE.

Model Results-

The high frequency portion of the circuit was modeled for 12 electrodes. R_{ct} is the parameter associated with the transient change in impedance noted earlier. Figure 9 shows R_{ct} for one week of a particular test. Clearly, the parameter exhibits a two-state behavior dependent on current pulsing. Figure 10 shows the relationship between R_{ct} and site size. A significant decrease is noted between 400μm^2 and 800μm^2 and a more gradual decrease after that.

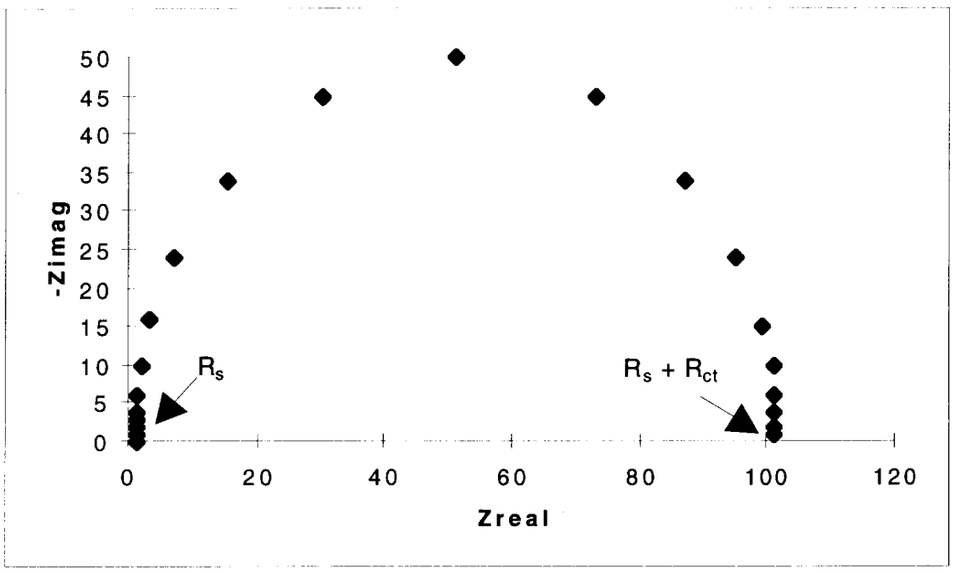

Fig. 7: Impedance Locus from Simplified Model

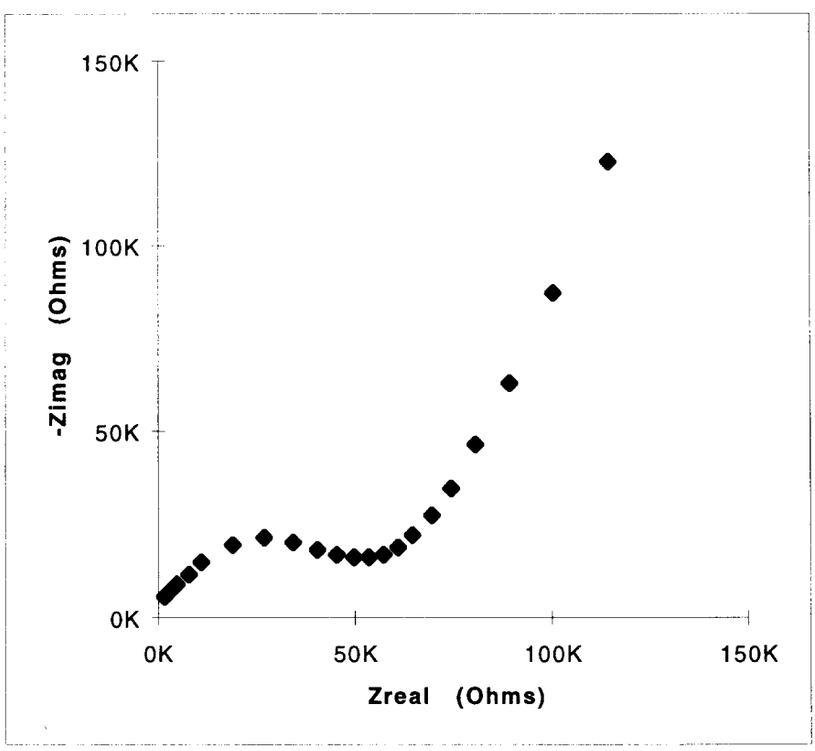

Fig. 8: Post Stimulation Impedance Locus

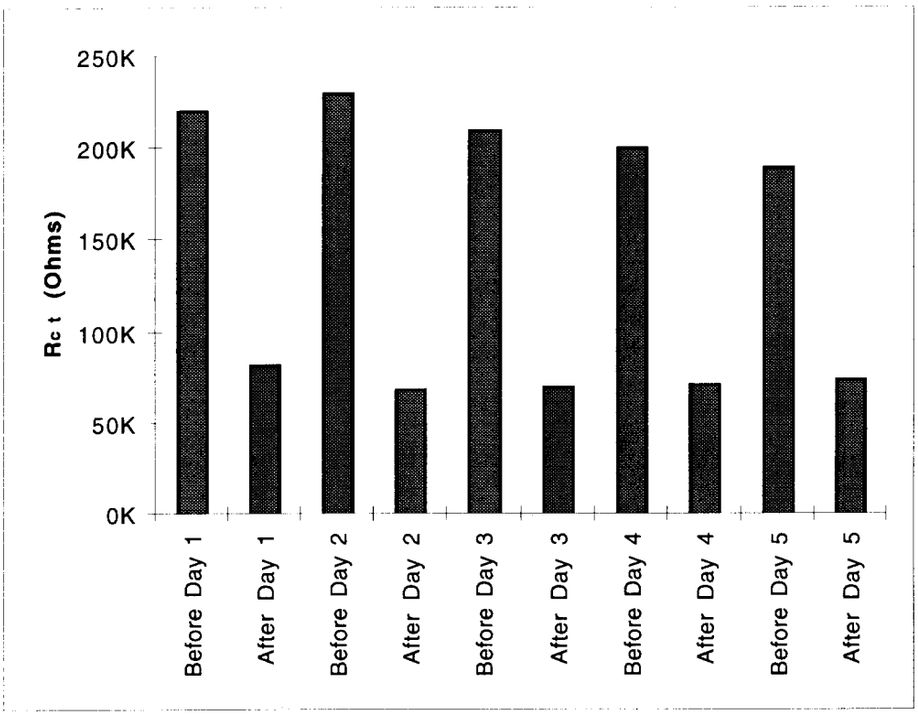

Fig. 9: Model Element R_{ct} for One Week of Stimulation

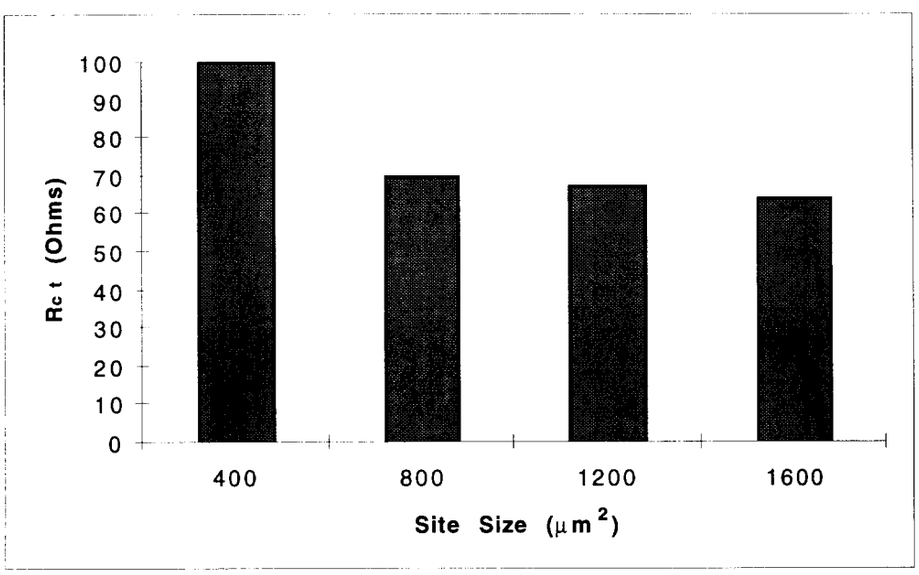

Fig. 10: Site Size vs. R_{ct}

It is theorized that current pulsing improves electrolyte access to the interface, thereby facilitating the oxidation/reduction reactions in the iridium oxide, resulting in a decrease in R_{ct}. This hypothesis is supported by *in vitro* tests that show no change in impedance when an electrode is pulsed in PBS. It has been suggested that a carbonate

buffered solution may provide a more realistic comparison to the in vivo environment. This will be investigated in the next quarter.

Electrode Characteristics in the Postoperative Period

An experiment was run to assess changes in electrode-tissue characteristics as a result of encapsulation and healing. A six-site probe was implanted and impedance and charge storage was monitored during the two week post-operative period usually allotted for implant recovery. No current pulses were applied during this time. Also, IS was done before and after CV testing, since it was noted that CV testing can affect the impedance (last quarterly report). Sites 1 and 6 were tested using both IS and CV and site 3 was tested using only IS. By day 3, impedance has increased significantly over post-op values (Fig. 11). Impedance magnitude before CV is high and somewhat inconsistent. CV testing lowers the impedance magnitude to a consistent level. Additionally, cyclic voltammagrams and charge storage remained stable throughout the two week period (Fig. 12). It was hoped that this animal could be sacrificed after pulsing to analyze the condition of the sites histologically, but the animal expired on the last day of testing. Another experiment of this type will be run in the coming quarter.

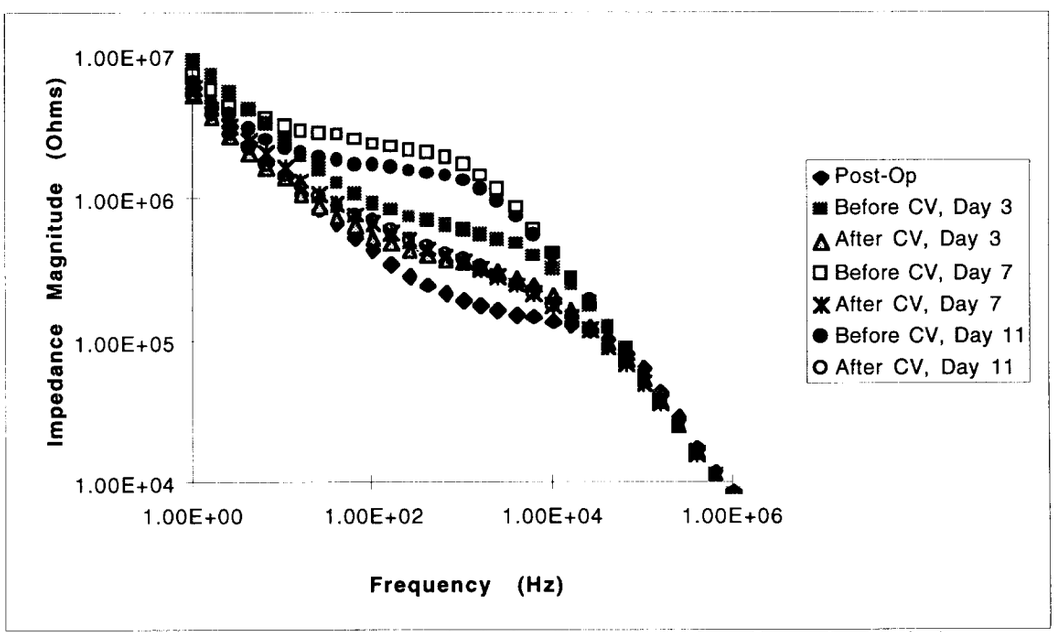

Fig. 11: Impedance Magnitude during Two Week Post-Operative Period.

Figure 13 summarizes the effects of CV and pulsing on impedance. CV testing seems to reset the oxide to a low impedance and current pulsing decreases the impedance even further. It is still unclear why back voltage doesn't decrease as dramatically as impedance (last quarterly report). The system is non-linear so comparing a small voltage perturbation to a large voltage excursion (10mV sine wave used in IS vs. 1V across the interface during pulsing) may not be valid. Also, the impedance decrease may occur in the first few current pulses. Some evidence to this effect was reported last quarter.

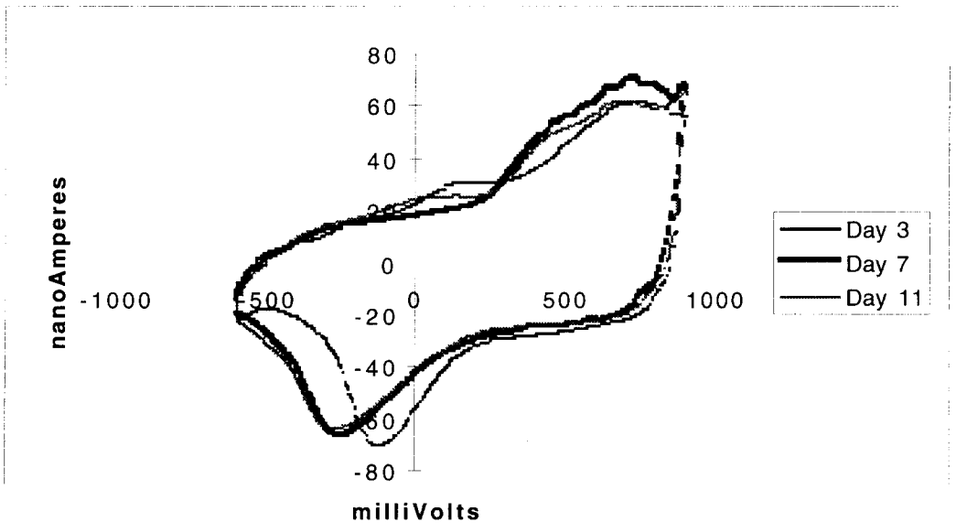

Fig. 12: CV during Two Week Post-Operative Period

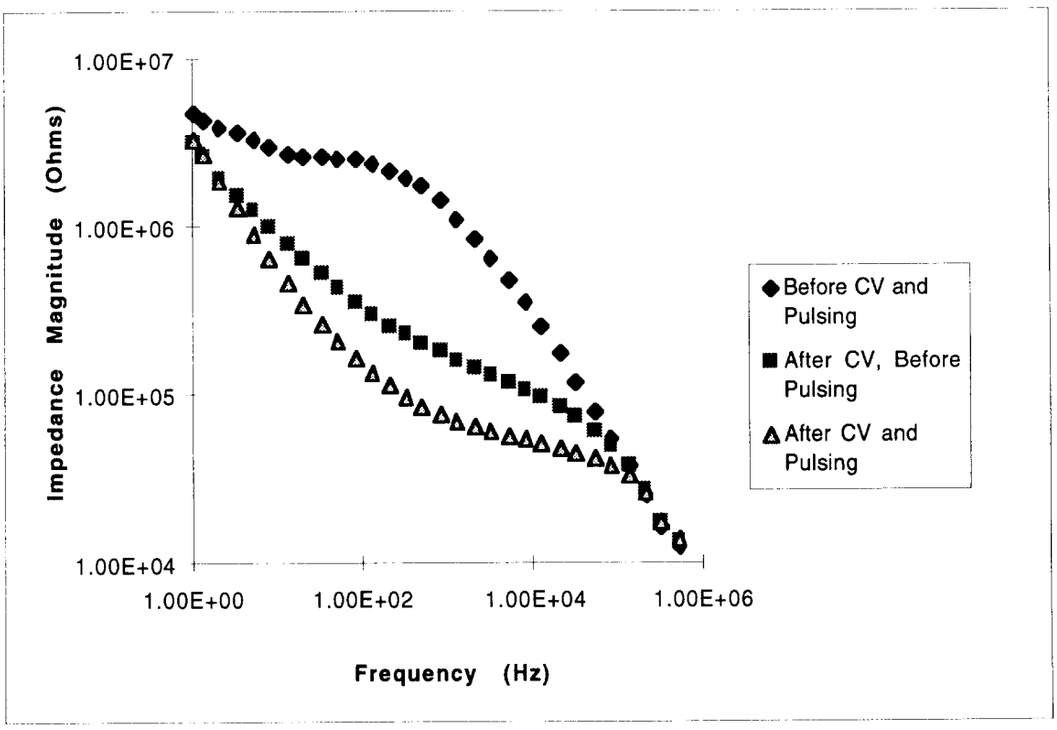

Fig. 13: Impedance changes due to CV testing and Current Pulsing

Modeling of data taken previously quantifies the current pulsing related impedance change noted in previous reports. The portion of the circuit model that is changing in response to pulsing is attributed to the Faradaic reactions within the iridium oxide. Encapsulation has a significant effect on impedance during the first two weeks of implantation. CV testing can partially reverse impedance increases.

Testing of New Electrode Site Design

Electrochemical testing of the new site structure has begun. Preliminary results from in vitro tests are shown below. Tests were run in PBS. These tests show that the new site structure results in a lower impedance everywhere except high frequency for both activated and unactivated electrodes (Figs. 13 and 15). Current pulsing (1.8 million pulses, biphasic 25μA, 100μsec/phase) had little effect on impedance magnitude. In general, the new sites activated more quickly (i.e., achieved a greater charge storage for a given number of activation cycles.) This may be due to the edges in the surface and the greater current density that will be seen at the edges.

We have seen open circuit potentials of -0.5 V vs. SCE on some of these electrode sites (typical OCP is about 0.2V vs. SCE). In the next quarter, we will run experiments on electrodes with different OCP's. Using electrochemical testing and SEM visual analysis, we will try to determine the source of the inconsistent OCP.

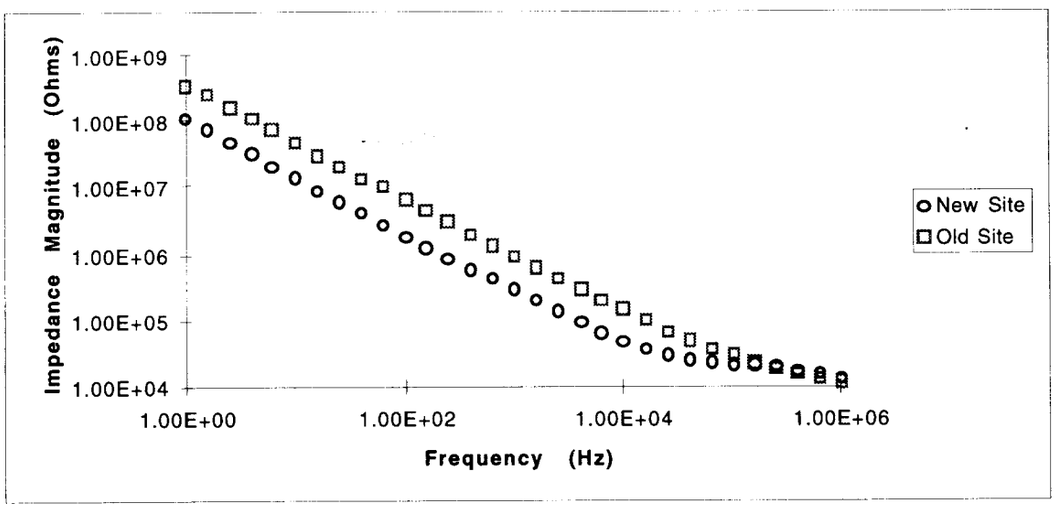

Fig. 14: New Site vs. Old Site, both 400μm², unactivated.

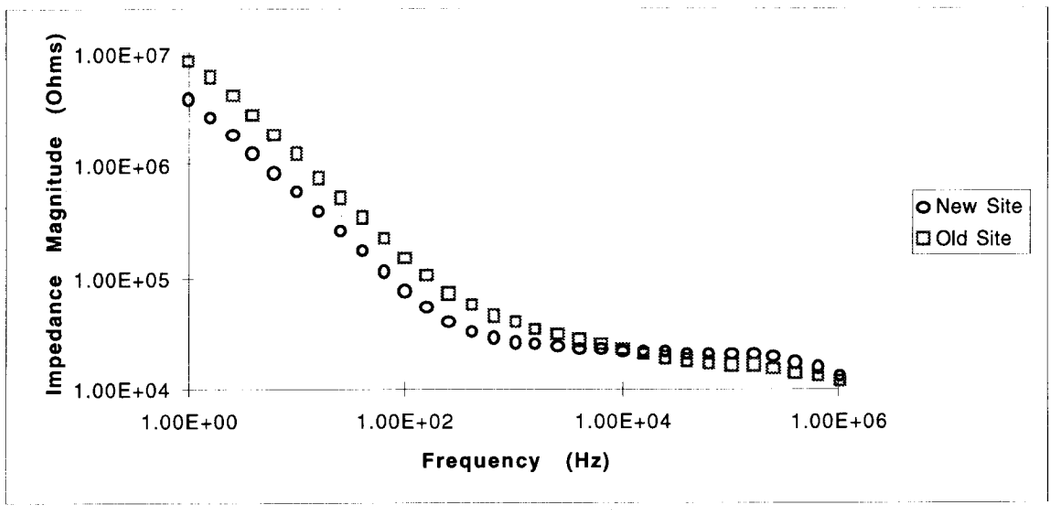

Fig. 15: New Site vs. Old Site, both 400μm², activated.

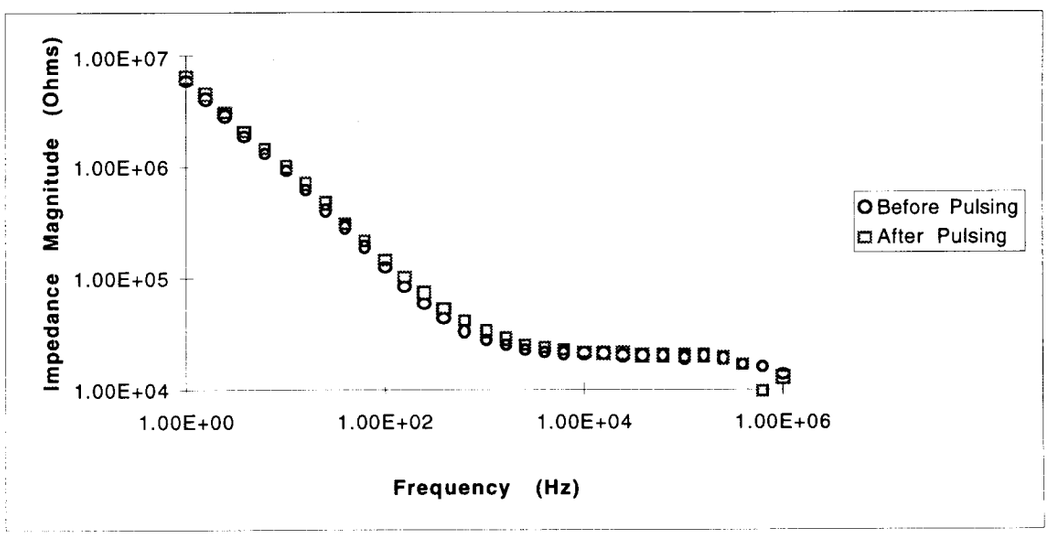

Fig. 16: 400μm² New Site, Before and After Current Pulsing.

During the next quarter, we hope to examine the histology from chronic experiments run this summer. In vitro testing of the new site structure will continue. Finally, another encapsulation experiment will be run and histology will be assessed immediately after stimulation.

4. Technology Development for Low-Resistance Interconnect

We have made marked progress over the past quarter toward our technology development goals. This includes work in both contact diffusion barriers and low-resistance, high-temperature interconnect. Contact diffusion barriers are used as a standard in industry to prevent a problem in integrated circuits known as junction spiking. When

two materials are in contact and have a tendency to interdiffuse, this can be very detrimental to contact properties. If, for example, silicon from a source or drain diffuses into an aluminum interconnect line, and aluminum diffuses into the silicon, the aluminum will short the source or drain to the substrate when it reaches the junction depth. By placing a material in the contact between the silicon and the interconnect which does not allow either material to diffuse into it, junction spiking is prevented. This intermediate material is known as a barrier or plug. A commonly used passive barrier, which allows no interdiffusion and does not degrade over time, is titanium nitride (TiN). A layer of Ti may be added between the silicon and the TiN barrier to reduce contact resistance, since Ti interfaces more intimately with both TiN and silicon than these two materials interface with each other. We have fabricated contact chains and Kelvin bridges using Ti-TiN-Al contacts to heavily doped silicon. All three metal layers were sputtered during a single pumpdown and patterned together, resulting in three layers over the entire interconnect pattern. This is in no way detrimental to the interconnect and avoids an additional lithography and sputtering step, which would increase contact area because of tolerance requirements. After liftoff, the wafers were annealed at 450°C for 30 minutes to form a more intimate contact between the metals, thereby reducing contact resistance. These contacts showed resistances of approximately 7.5Ω for 4μm x 4μm contacts and 10Ω for 3μm x 3μm contacts, which is not noticeably higher than resistances measured for contacts containing no barrier. Additionally, after the wafers were then annealed for 2 hours at 425°C, the temperature and approximate time required for a 1μm low-temperature oxide (LTO) deposition, the contact resistances remained low, even dropping several tenths of an ohm. This demonstrates that LTO may be used as a top dielectric over this type of interconnect without having a negative effect on the contact properties. An SEM photograph of a cross-section of one of the Si-Ti-TiN-Al contacts is shown in Fig. 17. The multilayered metal can be seen coming down over an insulating dielectric and making contact with the silicon substrate.

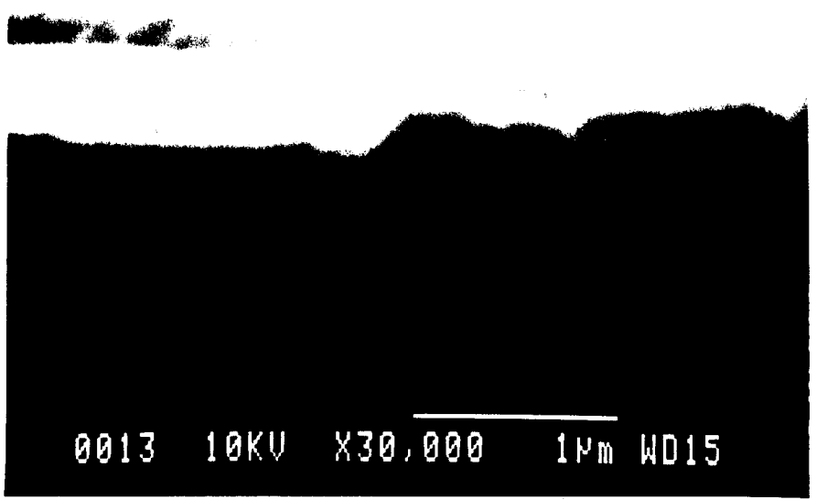

Fig. 17: This SEM photograph shows a cross-section of a Ti-TiN-Al interconnect line and contact to silicon. The multilevel metal can be seen running on top of an insulating dielectric, then coming down to make contact with the heavily doped silicon substrate.

SEM photographs of the contact chains used in these tests are shown in Fig. 18. In these chains, current flows through multiple contacts along a series of alternating metal strips and areas of heavily doped silicon. The resistance measured across the entire chain includes the contact resistances, as well as the sheet resistances of the metal and silicon, which must be subtracted out.

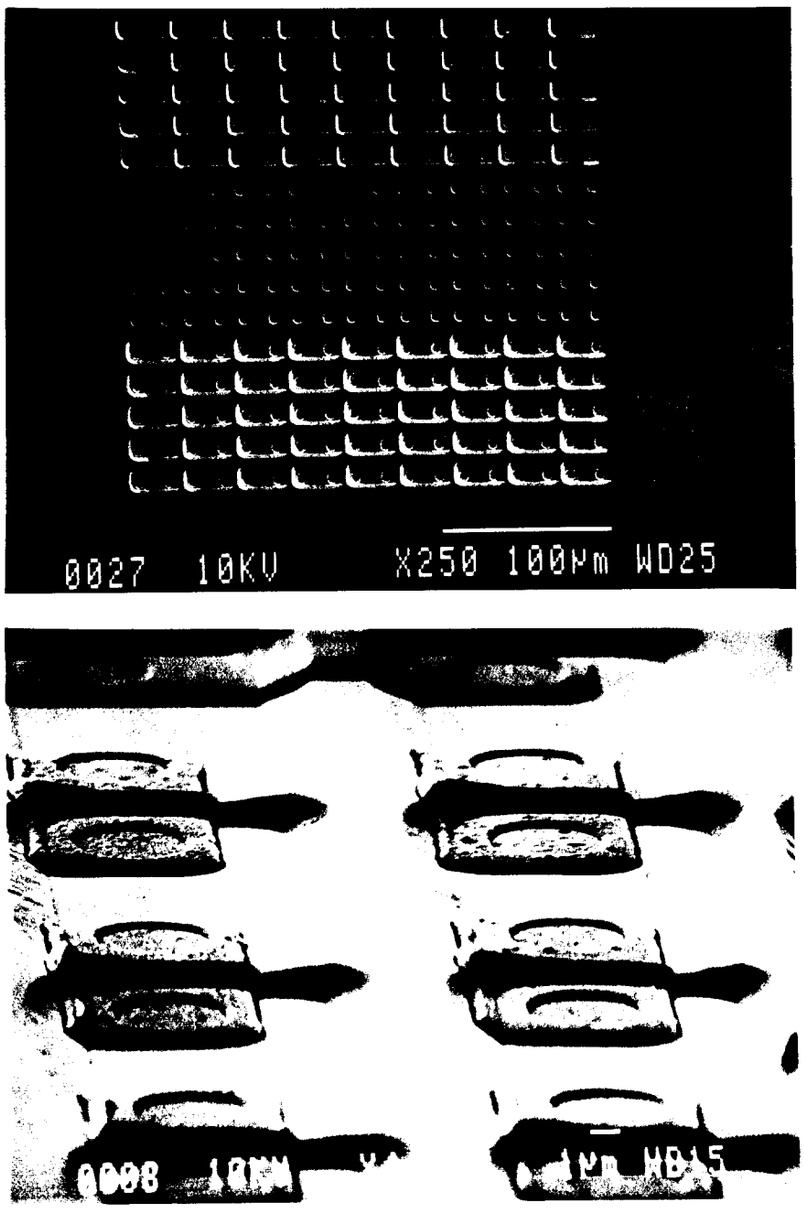

Fig. 18: SEM photographs of a contact chain used to test contact resistances between Ti-TiN-Al interconnect and heavily doped n-type silicon. These structures, as well as the masks used to pattern them, were fabricated in-house.

The low-resistance interconnect process being developed is currently also exploring tantalum silicide ($TaSi_2$) as the interconnect material. $TaSi_2$ is deposited by co-sputtering Ta and Si, then annealing to form a silicide and lower its sheet resistance. The Ta:Si atomic ratio is controlled by the powers at which the two materials are sputtered. The higher the silicon content, the lower the material stress, but the higher its sheet resistance. Trials were done to determine the optimum relative sputtering powers to produce a material as low as possible in both sheet resistance and stress. Once these parameters were determined, additional trials were done to optimize the annealing time and temperature. A 10-minute anneal at 675°C to allow the Ta and Si to react to form a silicide, followed by a 30-minute anneal at 850°C, was found to produce the lowest sheet resistance (~2.2 Ω/square). Since $TaSi_2$ is able to withstand temperatures of up to 950°C, LPCVD oxide and nitride may be used as top dielectrics over the interconnect. Just prior to LPCVD deposition, a layer of PECVD or sputtered silicon nitride is deposited to prevent the highly reactive Ta from oxidizing all the way through during top dielectric deposition. We are also investigating the use of straight Ta as an interconnect, which would further decrease sheet resistance, while still allowing much higher temperature processing following metal deposition than is possible when aluminum is used as the interconnect material.

Thus, over circuit areas, the use of the Si-Ti-TiN-Al system insulated with successive layers of LTO, PECVD nitride, a metal shield, and a polymer looks appropriate. Over areas where metal shields are not possible and the highest quality inorganic dielectrics are required, the Ta or $TaSi_2$ with high-temperature upper dielectrics appears feasible. These systems will be explored in probes to be fabricated during the coming quarter.

5. *Active Stimulating Probe Development*

During the past quarter, work in the active stimulating probe area has concentrated on fabricating more STIM-1B and STIM-1A probes. Work on improving the circuit contact formation process has also continued, and the design and layout of the most recent active probe, STIM-2B, is also nearing completion.

During the past quarter, the fabrication of the STIM-1A, STIM-1B, and STIM-2 probe set has continued. It was anticipated that the current run would be completed within the past quarter; however, laboratory equipment problems delayed their completion. These problems involved recurring gas alarms on our CVD furnaces. The cause of this problem has been identified and corrected. No further problems of this nature are expected. In addition, it should be stated that the LTO furnace installed during the past quarter is now fully characterized and operational for use in probe fabrication. This marks a major addition to our fabrication facility and to our capabilities for fabricating active stimulating probes.

Figure 19 shows a picture of one of the STIM-1A probe circuits in its current state of fabrication. The process is ready for gate oxide growth and polysilicon gate deposition. As noted in earlier reports, the development of both STIM-1B (our 16-site monopolar probe) and STIM-1A (our 16-site bipolar probe) are considered complete. The circuitry has been completely tested and found to be fully functional with performance near the targeted levels. However, more fully-functional probes are needed in order to support in-vivo characterization experiments planned for later this year. Hence, the present fabrication run is intended to provide these devices as well as additional experience with the probe process internally.

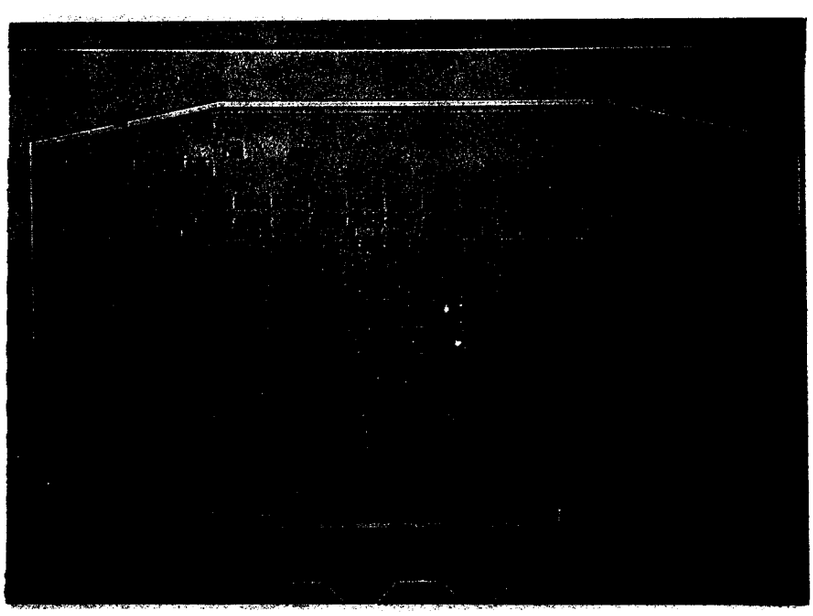

Fig. 19: A photograph of the circuitry of a STIM-1A probe as it appears in current state of the process. It is ready for gate oxide growth and polysilicon gate deposition.

STIM-2B is a second-generation four-channel 64-site version of the simplest active stimulating probe, STIM-1B. The circuit schematic of STIM-2B is shown in Fig. 20. The probe uses a 20b shift register to load four 4b addresses which are decoded to select one of sixteen sites per channel. The selected site is connected to the analog data input/output pad through a pass-gate transistor to allow externally generated currents to be 'steered' to the selected site. A flag bit is included with the channel address in order to select between stimulation and a newly added recording function. The flag bit selects either a direct path between the I/O pad and the site or selects the path through a buffer amplifier for recording. A power on reset circuit (POR) sets all of the circuits to a startup state and connects all of the sites to the I/O pads in order to facilitate activation of all of the sites in parallel. The first clock pulse knocks down the POR signal and the probe subsequently begins functioning normally. The POR state can also be initiated by strobing the clock line low, CSTB. A strobe on the address line, ASTB, resets all of the addresses to site zero and clears the flags (stimulation mode). Additional circuitry is included with site zero so that if the address line is held low, ASTB is maintained and all sites are disconnected thereby allowing the probe leakage current to be measured. The functionality of this device is dependent mainly on the correct operation of the digital logic circuitry for selecting the correct site for current delivery or recording. The recording buffer amplifiers are essentially the only analog circuits. The minimal amount of analog circuitry makes the design very robust with regard to dependence on process parameters.

The layout of STIM-2B, shown in Fig. 21, is nearing completion. Most of the major circuit blocks have been completed, including the 1-of-16 decoder, the bank of 16 site-access pass gates, the 20b shift register, and the amplifiers. All that remains is to layout the bank of level-shifters and several small miscellaneous circuit blocks and to then do the final global block placement and interconnections. It is estimated that the final circuit layout should be no more than about 7 mm^2 in size. The main block of circuitry per channel is the 1-of-16 decoder and the site-access passgates. This block, shown in Fig. 22, is essentially the same as that of STIM-1B except for the optimization of certain features and increases in the device separations in some areas to give a bigger margin of safety when operating with ±5V supplies. Completion of this layout is anticipated within the first month of the coming quarter. We will then complete modifications of STIM-2 to correct minor problems identified with this circuitry (primarily the weak pull-down of the n-channel DAC) and will lay this device out in a low-profile version consistent with use in 3D arrays. These devices will then be fabricated early in 1997.

Circuit Contacts

In the past, contacts have caused significant problems in realizing reliable fully-functional circuits. This has been attributed to various causes, including polymer formation, low surface doping densities (contacts not ohmic), and surface damage; all of these are associated with dry etching of the contact vias (RIE). Attempts have previously been made to circumvent these problems by using an O_2 plasma etch in the RIE after the normal oxide etch, buffered HF dips prior to metal deposition, and anneal steps after contact formation. These have, in general, been successful but additional improvements are nonetheless desirable to achieve the yields which this process should deliver. Based on an extensive literature study, we have compared the following methods for forming contacts. All of them use reactive ion etching (RIE) as the basic etch method followed by some type cleaning step:

1) RIE only
2) RIE followed by a buffered hydrofluoric acid (BHF) dip
3) RIE followed by a wet descum agent, NOE
4) RIE followed by a wet descum agent, EKC 265

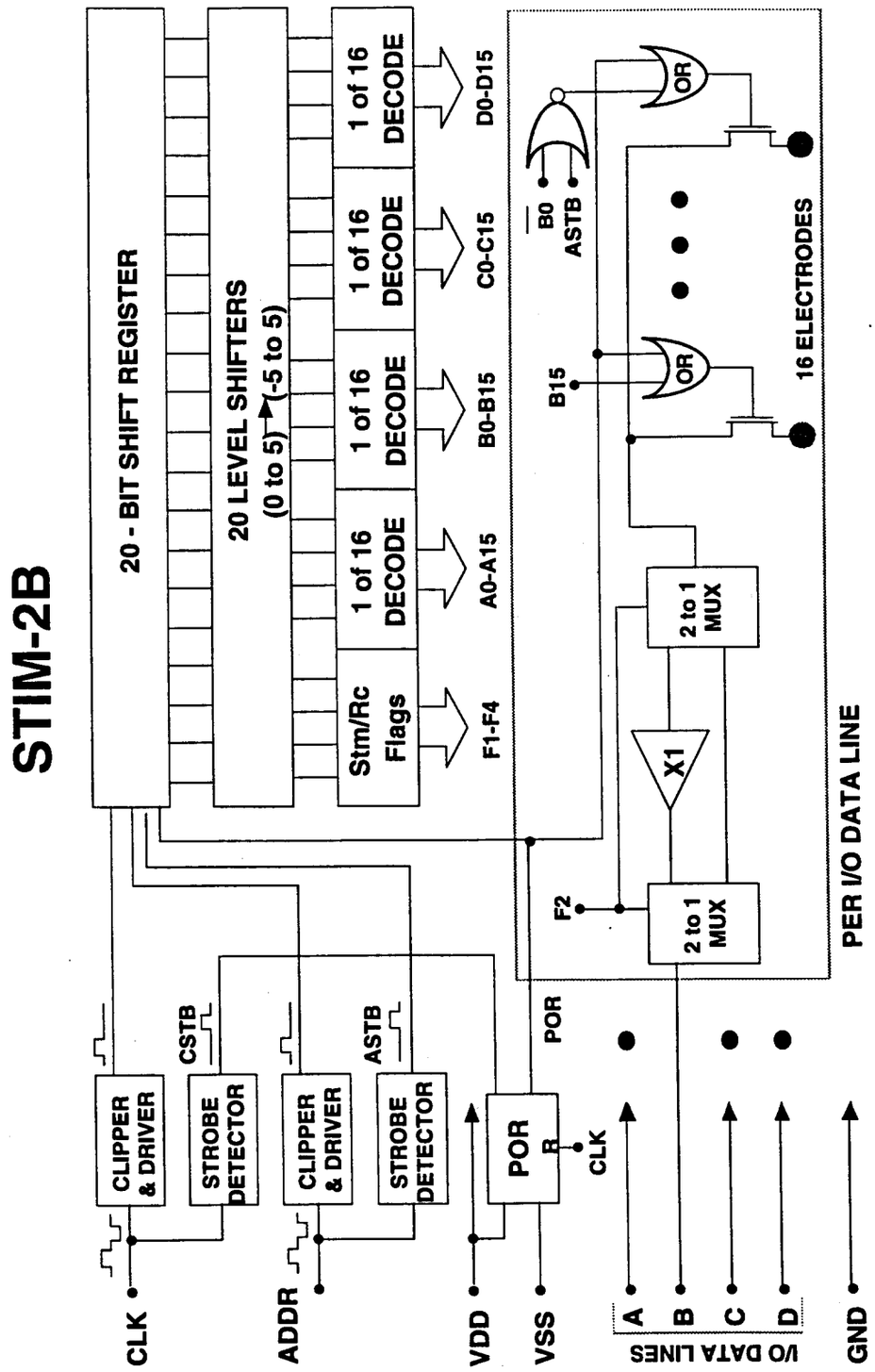

Fig. 20: Block diagram of the STIM-2B probe.

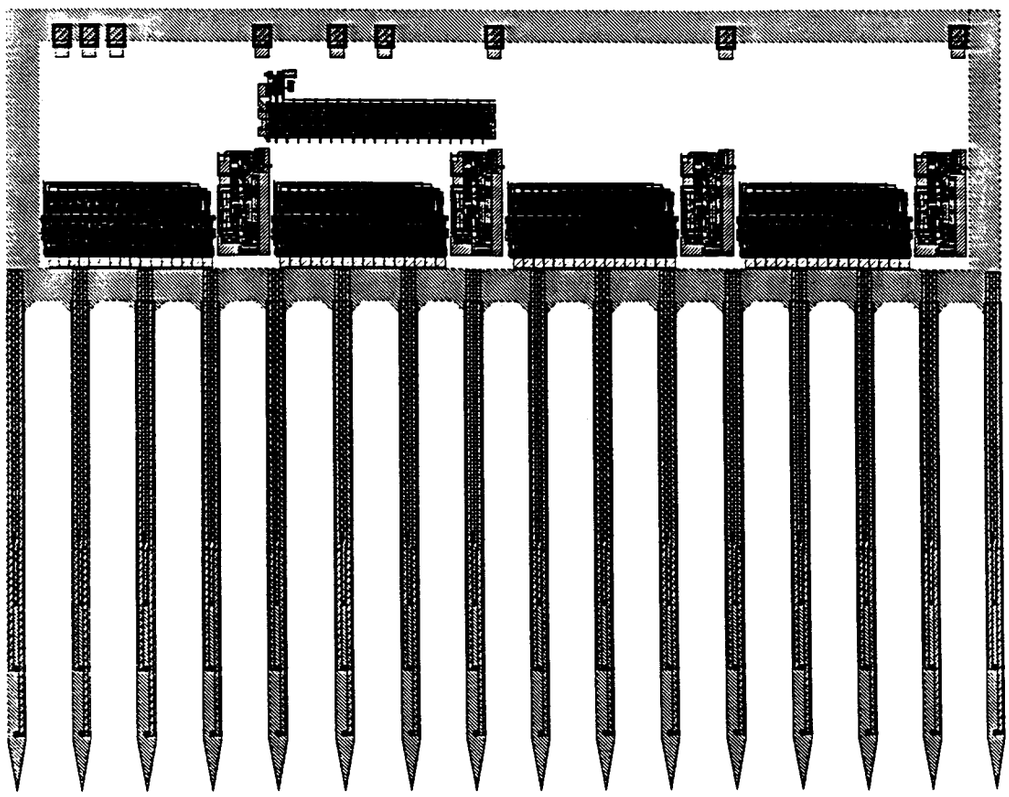

Fig. 21: The layout of STIM-2B (underway).

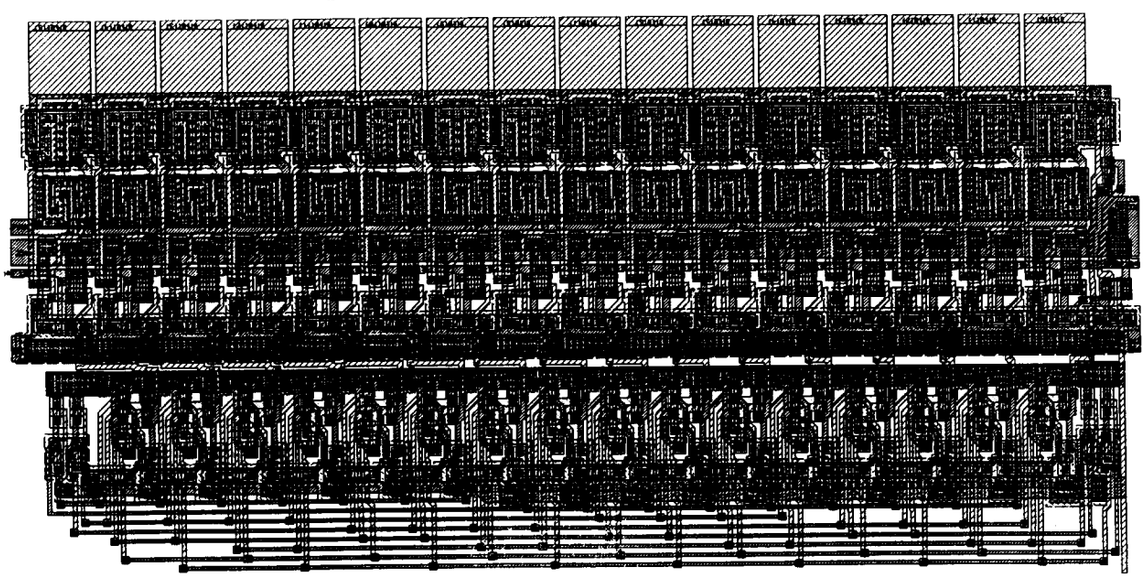

Fig. 22: The STIM-2B main per-channel circuit block, which includes the 1-of-16 decoder and the bank of 16 site access passgates.

5) RIE followed by a 400°C, O_2 anneal and subsequent BHF dip
6) RIE followed by a piranha clean

As a control, contacts were also formed by wet etching in buffered HF (BHF). This method is assumed to leave no residue in the contact opening; therefore, it should form the best contact. Unfortunately, this method is difficult to use in forming actual circuit contacts because the isotropic nature of the etch results in large lateral etching of the contacts under the masking photoresist which can lead to the possibility of circuit shorts. It is also difficult to use with oxide-nitride stacks.

The results of the work completed thus far are summarized in Fig. 23. Aluminum was the contact metal in all cases, and more processing details were given in the previous report. This figure excludes the 'RIE only' contacts to p+ silicon, which produced contract resistances in the 10's of kΩ's. Such contacts could clearly cause serious problems in probe circuit fabrication. They are known to have caused problems in site formation as well due to polymer residues left in place over the silicon. This study has confirmed that they also cause problems in circuit areas contacted by aluminum and indicates that the problem is particularly serious over p+ areas. Contact resistances to n+ polysilicon, to n+ source/drain (S/D) regions, and to p+ S/D regions are shown in Fig. 23. The resistances were measured across contact chains of 90/100 contacts.

While these results are based on limited experiments, they are nonetheless informative. The wet etched contacts are best to n+ polysilicon (better than any others produced) and are worst over n+ areas. This makes some sense; aluminum is a p-type dopant for silicon and can experience difficulties making contact to n-layers if the n-layer doping is not high enough. This can especially be a problem after long anneal steps; the use of an interfacial barrier (e.g., TiN) as discussed earlier should correct this problem. Neither RIE+BHF nor RIE+NOE does a good job on p+ silicon, presumably due to the inability to remove interfacial polymers adequately. The use of RIE plus an oxygen plasma does much better, and is known to remove polymers if the oxygen etch is vigourous enough. It is of some interest that we recently demonstrated a sensor for monitoring RIE polymer buildup that permits the evaluation of oxygen-plasma polymer removal as well. This may help to alleviate such problems in the future, both in our laboratory and in the industry in general. The RIE+Piranha (sulphuric-peroxide) sequence is also very good. This cannot be done in the presence of photoresist but has been the method used on the passive probes of late with the new non-self-aligned site structure. Thus, we find that both the RIE-Oxygen plasma and the RIE-Piranha techniques offer appropriate contact sequences. The others are not suitable for use on probe circuit areas.

During the coming quarter we anticipate completing the current CMOS process run of STIM-1A, -1B, and -2 probes. We also plan to complete the layout of STIM-2B and will begin the design and layout of three-dimensional active arrays built around the modified STIM-2 and featuring multiples of 64-sites up to a maximum of 1024 stimulation sites and 128 simultaneously-active channels.

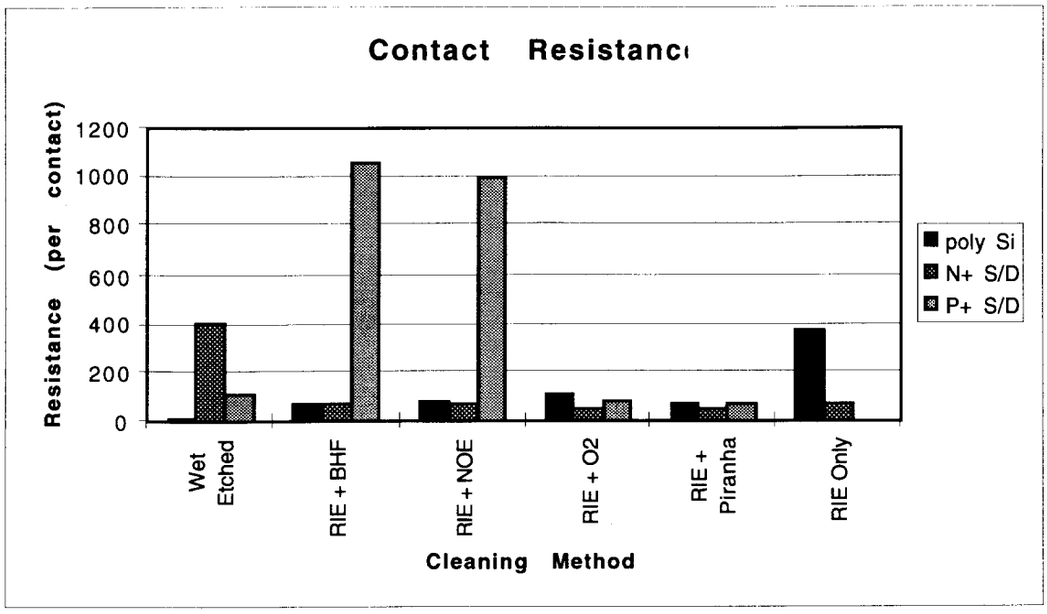

Fig. 23: Summary of contact resistances using different cleaning methods.

6. *An External Interface to Active Stimulating Probes*

We are in the process of designing a next-generation external electronic system for use with the active probes that will offer several improvements over the present design. The main goals are a higher sustained bit rate (10MHz), a flexible and on-the-fly-programmable probe communications protocol, and lower overall system complexity. We anticipate that these changes will allow the new design to be upwardly compatible with a wide variety of new probe designs.

The initial design for this new system was realized as a stand-alone self-powered unit that was connected to a host computer via a standard RS-232 serial line interface. These aspects of the design have not changed, but there have been some changes to the internal blocks of the new design as a result of an investigation into the existence and availability of special-purpose components.

The current design proposal for the new system is diagrammed below in Fig. 24. One of the major changes in the design is the replacement of separate memories for the on-board microcontroller and the memory for storing probe communication sequences by a single dual-port memory component. This single dual-port memory component not only reduces the amount of control circuitry required but also increases the range of possible probe communication protocols. This change also simplifies the microcontroller software development as the communications protocol memory can be mapped to any location in the microcontroller's memory space.

Another change in the design involves replacing the current probe voltage driver circuitry, currently implemented using analog switch integrated devices, with more flexible discrete circuitry. This circuit component is responsible for converting the binary-valued logic of the input signals to the ternary-valued logic expected by the probes. The problem

with the analog switch devices is that their output voltage range is limited. For greater flexibility in driving new probe designs, we wish to allow a greater range of output voltage. As there are no known analog switch integrated devices with a greater voltage range, a discrete-component analog switch implementation may be required.

We hope to complete the design of the new interface during the coming quarter and start construction of this system for use with the next run of STIM-2 and STIM-2B devices.

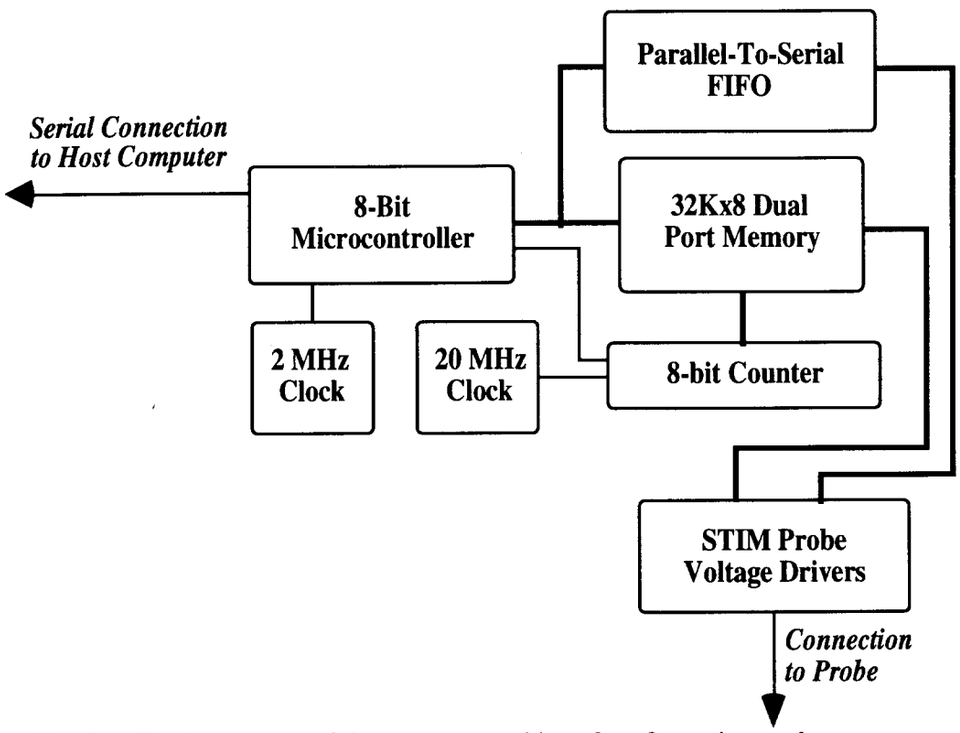

Fig. 24: Block diagram of the new external interface for active probes.

7. *Conclusions*

During the past quarter, work in this program has gone forward in several areas. We have continued to fabricate passive probe structures for internal and external users. These probes have used the new site design, which allows the site to overlap adjacent conductors and permits a thorough cleaning step after via formation and before metal. Passive probes have been successfully fabricated using an external foundry (MCNC, Research Triangle Park, NC) as an effort to improve yield on devices where the fabrication process and designs are fully developed. The resulting probes appear very good, with dielectric stresses near neutral and interconnects well defined and defect free.

Results of in-vivo site pulsing have been interpreted in terms of an equivalent circuit model, focusing on the range between 100Hz and 10kHz. The impedance magnitude

spectra agrees well with the model. Changes due to current pulsing can be correctly modeled in terms of the charge-transfer (redox) reactions thought to occur within the iridium oxide. It is theorized that current pulsing improves electrolyte access to the interface, thereby facilitating the oxidation/reduction reactions in the iridium oxide. This hypothesis is supported by *in vitro* tests that show no change in impedance when an electrode is pulsed in PBS. Encapsulation can be observed in these impedance spectra and has a significant effect on impedance during the first two weeks of implantation. CV testing can partially reverse these impedance increases, implying, for example, that the ability to stimulate recording probes to improve their electrolyte access should be beneficial. The impedance spectra of the new site structure are not significantly different than those of the older structure, although anomolous open circuit potentials have been observed on some sites and are being studied.

The use of TiN plugs in circuit vias has been successful. These Si-Ti-TiN-Al contacts showed resistances of approximately 7.5Ω for 4μm x 4μm contacts and 10Ω for 3μm x 3μm contacts, which is not noticeably higher than resistances measured for contacts containing no diffusion barrier. Additionally, after the wafers were then annealed for 2 hours at 425°C (the temperature and approximate time required for a 1μm low-temperature oxide (LTO) deposition), the contact resistances remained low, demonstrating that LTO may be used as a top dielectric over this type of interconnect without any negative effects on the contact properties. $TaSi_2$ has also been explored as an interconnect in areas requiring high-temperature probe upper dielectrics (e.g., on probe shanks). This material has been found to allow resistances of abourt 2.2 ohms/square (five times less than polysilicon) and is able to withstand temperatures of up to 950°C, consistent with the use of stoichiometric LPCVD oxide and nitride top dielectrics.

Studies of contact formation etch techniques have concluded that the use of RIE plus either an oxygen plasma or a piranha etch to remove residual polymers can produce high-quality contacts over both n- and p-type silicon and polysilicon areas. The use of RIE alone or RIE plus BHF or other chemical cleaning agents has not been found to be acceptable with all surfaces to be contacted. Work on the development of active probes is continuing and will use these new contact and interconnect structures. A new run of STIM-1A, -1B, and -2 probes is now underway. In addition, the layout of STIM-2B, a four-channel 64 site probe with off-chip current generation, is nearing completion.